

High-Performance Quadrature Modulators for Broadband Wireless Communication

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Abstract -- A quadrature modulator operating from 250-1000 MHz, having a maximum output level of +3 dBm into a 50-ohm load and a noise floor of -155 dBm/Hz has been developed. The device draws 65mA from a single 2.7 to 5.5V supply when active, and 70uA during standby. The high dynamic range achieved by this device is attributable to the design of its baseband interface, as well as its complementary bipolar process with insulated substrate. A high frequency version of this chip provides similar performance from 800-2700 MHz.

I. INTRODUCTION

A. Digital Modulation Systems

Modern communication systems employ various forms of quadrature modulation to maximize the amount of information transmitted through a communication channel. Third-generation (3G) cellular systems use the Wideband Code Division Multiple Access (W-CDMA) [1] format, sending data from up to 60 users within a 5 MHz channel. Each user's data is identified by a different pseudo-random code modulating the data using Quadrature Phase-shift Keying (QPSK). Next generation fixed wireless access systems such as Local Multipoint Distribution System (LMDS) [2] are being designed with more complex modulation formats to attain greater data rate, typically moving from QPSK to more multi-level modulation. LMDS implementations do not share a common standard across vendors, but these systems often employ 64- or 256-QAM (Quadrature Amplitude Modulation) formats, transmitting data at several million symbols per second.

Traditionally, data is first modulated on to a low Intermediate Frequency (IF) carrier, and then up-converted to the final frequency using multiple Local Oscillators (LO), mixers and filters. Modulators that operate directly on a high-frequency carrier will reduce system cost by eliminating these intermediate stages. A functional block diagram of a direct conversion

modulator for these digital communication systems is shown in Fig. 1.

B. Survey of Monolithic Quadrature Modulators

Various monolithic RF quadrature modulators have been reported in the literature, with several also available as commercial components [3-6]. Table 1 summarizes the reported performance of some of these devices including the AD8346 [3], which is the predecessor of this work.

Since the AD8346 was introduced, it has rapidly found applications in cellular basestations. As cellular systems move into their third-generation designs, a modulator with higher dynamic range has been called for. The techniques described here were developed to meet this requirement.

II. GOALS

A. Frequency Range

Two monolithic integrated circuits have been developed to cover the frequency ranges used by different radio systems. The IF modulator operates from 250 to 1000 MHz, which includes many popular IF frequencies for cellular systems, in addition to the 900 MHz cellular band itself. The RF modulator covers 800-2700 MHz, which includes all the cellular

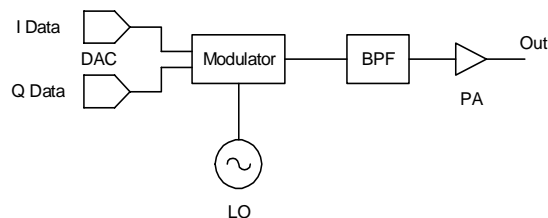


Fig. 1 Direct conversion modulator block diagram

TABLE I
PUBLISHED QUADRATURE MODULATOR PERFORMANCE

Device	Freq. (GHz)	P1dB (dBm)	SB Suppression (dBc)	Noise Floor (dBm/Hz)	Output Level (dBm)	ACLR* (dB)
AD8346 [3]	2.1	-6	-35	-147	-21	60
Itoh (1999) [4]	2.1	N/A	<-40	N/A	-14	60**
RF2480 [6]	2	-3	N/A	-158	-17	N/A
IF Modulator	1	3	-44	-155	-10	60
RF Modulator	2	-1	-35	-156	-14	60

* W-CDMA

** QPSK @ 4 Mchips/s

and Personal Communication Systems (PCS) frequencies, as well as the IF frequencies used in LMDS systems.

B. Sideband Suppression

When a modulator is configured for single-sideband modulation, undesired sideband suppression provides a measure of phase quadrature accuracy as well as amplitude balance between the In-phase (I) and Quadrature-phase (Q) channels. The sideband suppression goals (over process and temperature variations) of the IF and RF modulators are -40 and -35 dBc, respectively. These are the practical limits set by on-chip component matching, without resorting to more complicated methods of calibration.

C. Dynamic Range

The dynamic range for a modulator can be expressed in terms of the difference between its output 1-dB compression power level (P1dB) and broad band noise floor. The goals for this device are:

$$\begin{aligned} \text{P1dB} &> 0 \text{ dBm} \\ \text{Noise floor} &< -150 \text{ dBm/Hz} \end{aligned}$$

III. ARCHITECTURE

Both modulators share the same architecture shown in Fig. 2. Each device is divided into the following sections: Local Oscillator (LO) Interface, Baseband Differential Voltage-to-Current (V-to-I) Interface, two Doubly-balanced Mixers, Output Differential-to-Single-ended (D-to-S) Converter, and Bias Generator.

The LO Interface generates two carriers at 90 degrees of phase difference with each other, to drive the two mixers in quadrature. The baseband signals are converted into current form in the Differential V-to-I Converters, for feeding into the two mixers. The outputs of the mixers are summed together before being passed to the D-to-S Converter, which provides a 50-

ohm output interface. Bias currents to each section are controlled by an Enable signal. Detailed operation of each section is described below.

IV. CIRCUIT DESCRIPTION

A. LO Interface

The LO Interface consists of interleaved stages of polyphase phase-splitters and buffer amplifiers. The polyphase phase-splitter (Fig. 3) contains sets of resistors and capacitors connected in a circular manner so as to split the LO signal into I- & Q- paths in precise quadrature with each other. The signal on each path is applied to a buffer amplifier to make up for the attenuation and high frequency roll-off. The two signals are then fed to another polyphase network to enhance the quadrature accuracy. Broad operating frequency range is achieved by staggering the R-C time constants in each stage of the phase-splitters. The outputs of the second phase-splitter are applied to the driver amplifiers for the mixers' LO inputs.

B. Differential V-to-I converter

In this circuit, each baseband-input pin is connected to an op-amp driving a transistor connected as an emitter follower. A resistor between the two emitters maintains a varying current proportional to the differential input voltage through the transistor. These currents are fed to the two mixers in differential form. The mixer currents are thus linearly proportional to the baseband-input voltages, eliminating one common source of distortion in modulators.

C. Mixers

There are two Gilbert-cell doubly balanced mixers, one for the In-phase Channel (I-ch) and one for the Quadrature Phase Channel (Q-ch). The output currents from the two mixers are summed together in two load resistors. The signal developed across the load resistors

is sent to the Differential-to-single-ended output converter. The size and base voltage drive of the mixer transistors are optimized to produce crisp edges as the baseband currents are being switched by the LO signal.

D. Differential-to-Single-ended Output Converter

The differential-to-single-ended output converter consists of two emitter followers driving a totem-pole output stage (see Fig. 5). Output impedance is established by the emitter resistors of the output transistors. The output of this stage is connected to the output (VOUT) pin.

E. Bias Generator

A bandgap reference circuit based on the ΔV_{BE} principle generates the Proportional-To-Absolute-Temperature (PTAT) currents as well as temperature-stable currents as needed by the different sections. When the bandgap reference is disabled by pulling down the signal at the Enable pin, all other sections are shut off accordingly.

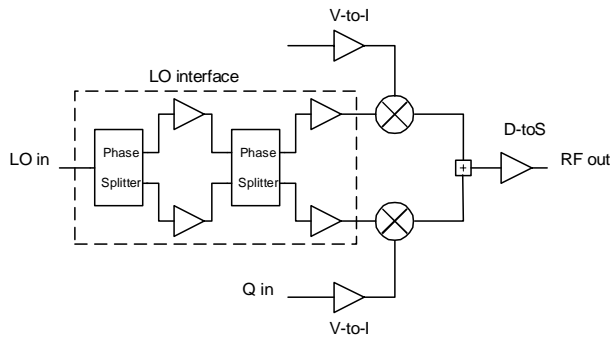


Fig. 2 Quadrature Modulator Block Diagram

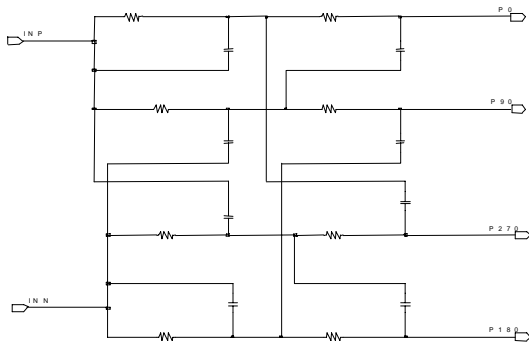


Fig. 3 Polyphase Phase-splitter

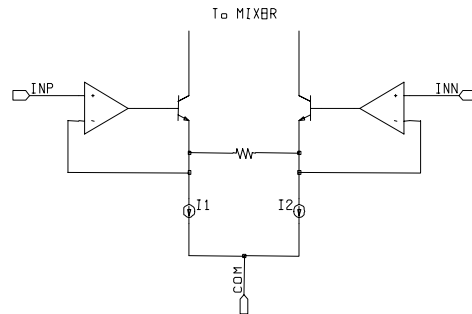


Fig. 4 Voltage-to-current converter

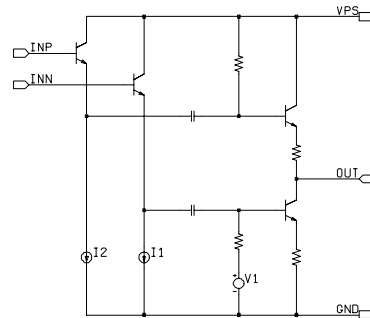


Fig. 5 Diff.-to-single-ended output converter

V. PERFORMANCE

A. Sideband Suppression and LO Feedthrough

Fig. 6 shows the sideband suppression and LO feedthrough of the two modulators over their respective frequency ranges. We can see that within their whole operating frequency range, the two modulators maintain 28 to 45 dB of sideband suppression, and less than -33 dBm of LO feedthrough at an LO input level of -2 dBm.

B. Dynamic Range

Output-referred P1dB levels of +3 and -2 dBm are achieved by the IF and RF modulators at 1 and 2 GHz, respectively. Broadband noise floor varies from -156 to -155 dBm/Hz over the full operating frequencies for both devices, exceeding the 150-dBm/Hz dynamic range goal set above by a satisfactory margin.

C. W-CDMA, Multi-carrier & 64-QAM Performance

The output spectrum of the RF modulator under

W-CDMA at 2 GHz with 15 codes plus pilot is shown in Fig. 7. An ACLR (Adjacent Channel Leakage power Ratio) of 55dB is achieved at an output level of -11 dBm.

Fig. 8 shows the RF modulator's ACLR performance at 2 GHz operating in 64-QAM, a format that is used by many microwave communication links as well as the Digital Video Broadcasting in Europe.

Output spectrum of the IF modulator with 10 NADC (North American Digital Cellular) carriers is shown in Fig. 9. High signal-to-noise ratio is maintained with low intermodulation distortion.

VI. CONCLUSION

Performance of the IF and RF modulators under different metrics have been presented. Both the IF and RF modulators provide excellent amplitude and phase balance, as indicated by their good sideband suppression performance. Coupled with their wide modulation bandwidth and large dynamic range, they enable the high data rate modulations of the next generation of communication systems at a low system cost.

ACKNOWLEDGEMENTS

This work would not have been possible without the continuous advice and encouragement by Dr. Barrie Gilbert and our colleagues at ADI. Special thanks are due to Sue Peinkofer for the layout, and Mike Chowkwanyan, Jim Martin, as well as Dana Whitlow for characterization.

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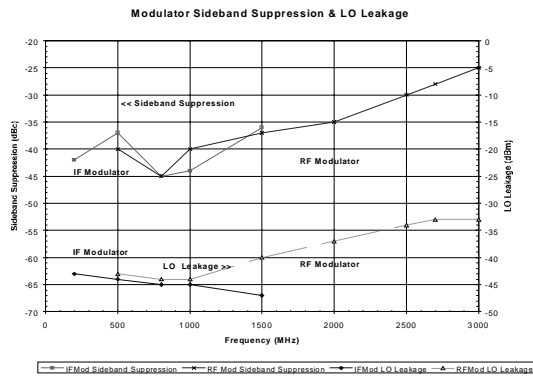


Fig. 6 Sideband Suppression & LO Leakage

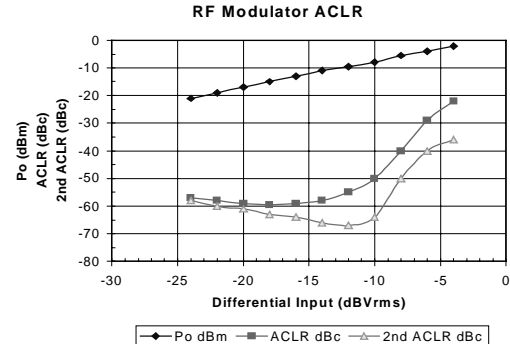


Fig. 8 RF Modulator ACLR

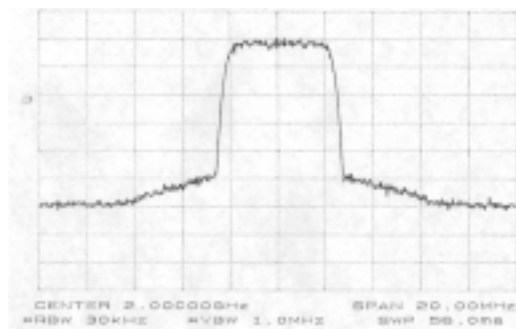


Fig. 7 W-CDMA output spectrum

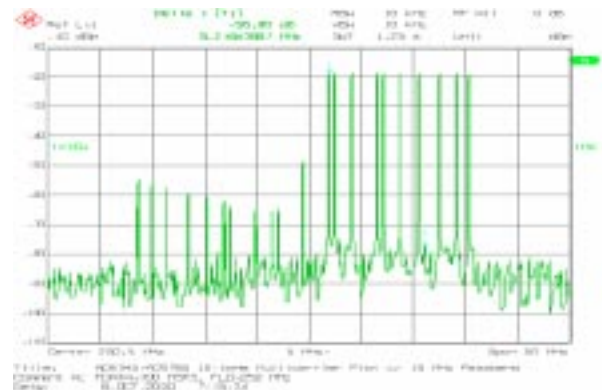


Fig. 9 IF Modulator Multi-carrier Output